TECHNICAL MEMORANDUM (NASA) 9

LOW-COST OMEGA NAVIGATION RECEIVER

The status of Ohio University's efforts toward specifying a low-cost Omega receiver is reviewed, at the onset of the fourth-year program under the NASA Tri-University Program in Air Transportation Systems.

by

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1. INTRODUCTION

This Technical Memorandum serves (1) to document the status of the Low-Cost Omega Navigation Receiver being designed and constructed by Ohio University for the NASA Tri-University Program in Air Transportation, (2) to serve as an introduction to the program for new project workers joining us in the fourth year effort (1974-75) and (3) to outline expected directions for the fourth year work.

In the Tri-University program, Ohio University has designed and constructed a flight-model Omega Receiver Base with front-end filter-gain module, timing modules and a memory-aided digital phase-lock loop (MAPLL) correlator. Design work is essentially complete for a frequency synthesizer based upon digital binary rate multipliers, which is soon to be evaluated as a receiver time-base generator. These results are presented in more detail in the appropriate sections of this paper. Some have been released during the third-year NASA program as Technical Memoranda and are cited specifically. Other results represent elements of work currently in progress and which will be the subjects of future reports and papers.

Emphasis is placed on the completion and testing of a modular, multipurpose Omega receiver which utilizes a digital memory-aided phase-locked loop to provide phase measurement data to a variety of applications interfaces. One such applications interface could condition the digital phase measurements for input to a microprocessor flight navigation computer. Another might provide basic Omega chart outputs for use in water navigation at lower speeds. Still another applications interface could provide appropriate signals for the generation of a differential Omega correction message, with the receiver in use as a ground monitoring station. Our objective is to build a low-cost, generalized receiver base from which data can be taken on the ground and in flight tests for later use in applications module development.

The receiver documentation contained in this paper describes the functional units contained in the prototype device. The receiver, containing less than $100 worth of integrated circuits in its present form, receives and stores phase measurements for up to eight Omega signals and computes two switch-selectable LOP's, displaying this navigation data in chart-recorded form.

As has been the case in the past, Avionics Engineering Center professional staff members, faculty consultants from the Department of Electrical Engineering, Ohio University, and student assistants, both graduate and undergraduate, are participating in the program.

II. OMEGA RECEIVER BASE

A. Introduction

Figure 1 shows the Ohio University Omega Receiving Station in use for evaluation of the flight model Omega receiver base. A Tracor 599-R receiver is used as the primary benchmark device. A Tracor 304B Rubidium frequency standard and a Sulzer 5-D frequency standard are available, along with frequency counters and other standard measuring equipment.

Two Omega receivers have been designed and constructed during the Tri-University program. Figure 2 shows the breadboard model of the Simultaneous-Omega-Pair receiver completed during the third-year effort. Figure 3 illustrates the current flight-model receiver base unit using digital phase-locked loop techniques in a single-frequency (10.2 or 13.6 KHz) mode.

In the following paragraphs, the present status of each module in the receiver base is discussed, along with proposed changes in design or implementation during the fourth-year Tri-University program.

The basis for some of the work documented here has been reported in R. W. Burhans', "Simplified Omega Receivers", Technical Memorandum NASA-4, Avionics Engineering Center, Ohio University, March, 1974. Excerpts from this earlier paper are included in the following pages, updated to reflect more recent work.

The receiver base uses TTL digital logic and bus-type backplane construction with functional modules on plug-in circuit boards. A modular power supply allows easy compatibility with aircraft electrical systems and with bench testing at 110V, 60 Hz power.

B. Antenna and Preamplifier

The transmitted OMEGA signals are derived from atomic clocks with very high precision in time and phase stability, synchronized with precision of ± 1 part in 10^{11} per day (about +1 microsecond per day errors). Ten KW and large transmitting antenna systems typically result in signal levels of 300 microvolts at 800 nautical miles across the input to a high impedance preamplifier with a short receiving whip antenna (20 foot wire). The atmospheric noise level at 10.2 to 13.6 KHz on a short wire antenna is typically quite high, approximately 1 microvolt/Hz of receiver bandwidth.

A short whip or wire antenna is by far the simplest to install but suffers from locally generated precipitation static in blowing snow or rain, and is non-directional with respect to nearby thundershower spherics and other local interference. A loop or crossed pair of loops can reduce local noise in many applications, but requires more processing for the

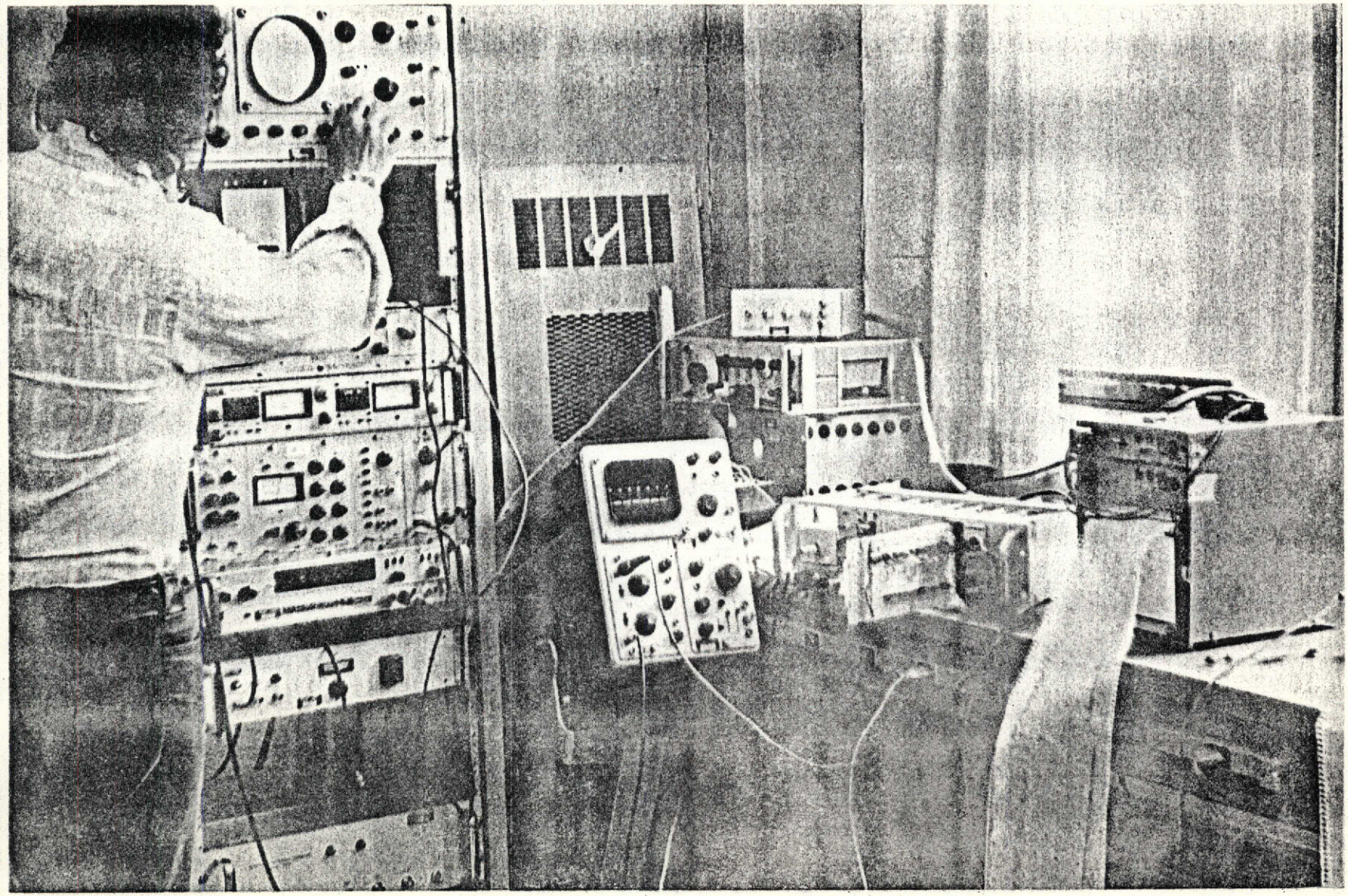


Figure 1. The Ohio University Omega Receiving Station Using Tracor 599R Receiver.

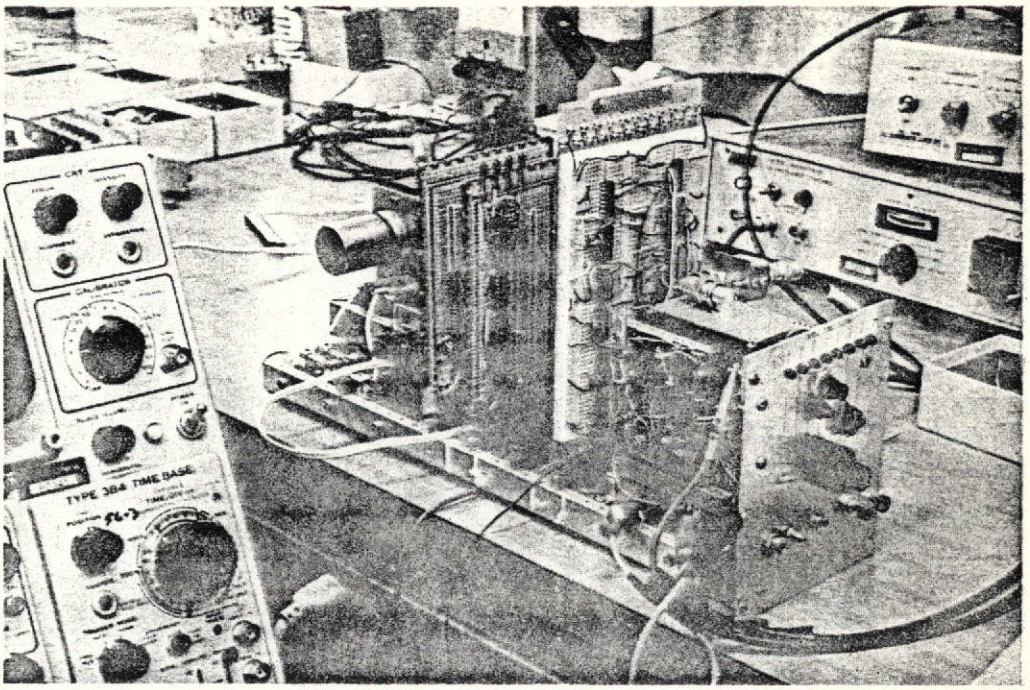


Figure 2a. Breadboard Model of Omega Receiver.

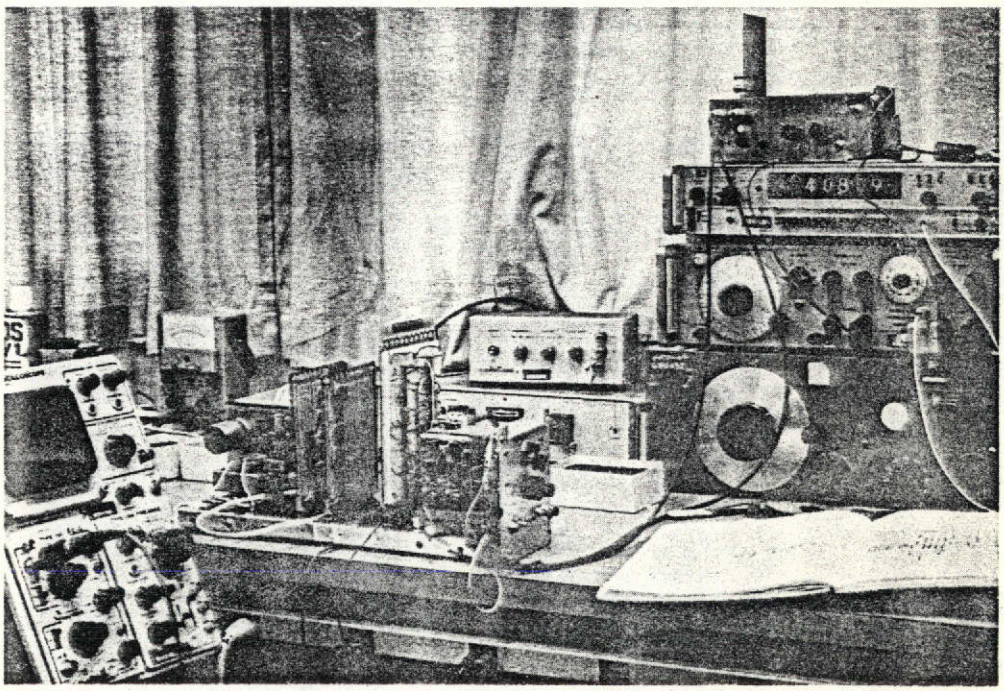


Figure 2b. Simultaneous Pair Omega Receiver Evaluation in Laboratory.

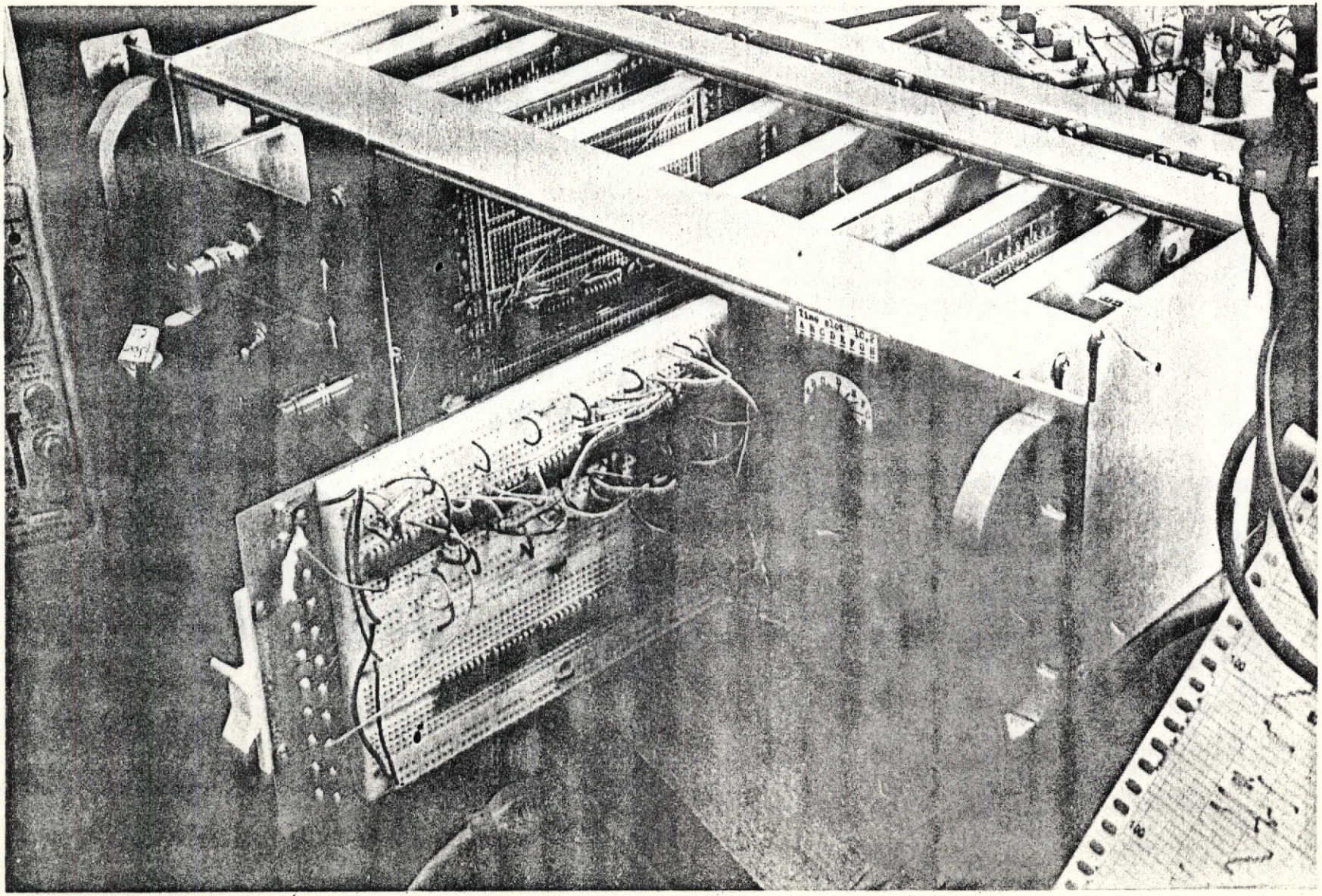


Figure 3. Airborne Omega Receiver Prototype Equipment Fabricated by Ohio University Avionics Engineering Center for Use in the NASA-Supported Tri-University Program.

phase ambiguity introduced depending upon the direction to the transmitting source. Much work has been done and many methods are proposed for reducing antenna noise problems, all of which tend to increase the cost of present receiver systems. A commercially available crossed loop antenna system for VLF can cost about $1000. If our goal is eventually a receiver -processor system for OMEGA with a total cost of less than $1000, some much simpler approaches to this problem are required. A single wire antenna appears usable in most cases if proper attention to the details of the preamplifier and filter assembly is given. It appears that improvements in noise level can be achieved through proper location of antennas above and below the aircraft and through appropriate combination of the signals from the two antennas.

A preamplifier with high input impedance is used with sufficient gain to overcome the noise of common operational amplifier networks applied to ceramic or mechanical high-Q bandpass filters. A preamplifier with a voltage gain of 10 (20 db) is desirable with an input noise factor less than 0.1 microvolt/Hz. An amplifier is obtained from a diode-protected dual gate MOSFET operated in the mode illustrated in Figure 4. Here the whip antenna is coupled through an isolating capacitor to the control gate, and the preamplifier is physically located at the antenna end. The MOSFET drives a transistor amplifier, transformer coupled through a wide-band transformer of the DIT variety. The low impedance output line from the transformer couples the signal to the receiver, and the 5-volt power for the preamplifier operation is supplied over the same cable.

Using an antenna and preamplifier as described above, signals from Omega stations B (Trinidad), C (Hawaii, now testing), D (North Dakota) and G (Forestport, New York; testing on most days) are available with sufficient strength to permit measurements to be made. We anticipate no significant changes to these components of the receiving system during the fourth-year program.

C. Receiver Front-End Modules

The front-end filter-gain module accepts signals from the antenna preamplifier and, in the prototype receiver base, produces outputs at both 10.2 and 13.6 KHz for later processing. Only a single output is planned in a final design, but the existence of both frequencies for development work will allow assessment of relative signal-to-noise characteristics at both frequencies, plus the possibilities of simultaneous Omega operation (See R. W. Burhans', "Simultaneous Master-Slave Omega Pairs", Technical Memorandum NASA-7, Avionics Engineering Center, Ohio University, April, 1974).

The low-Z output line of the preamplifier directly drives split-ring ceramic filters which operate like high impedance mechanically coupled tuning forks. These ceramic filter units are potentially available at quite low cost if sufficient demand for them in the VLF-OMEGA market can be created. A single filter unit followed by a gain block of 10 db results in the first stage bandwidth reduction of Figure 5. These filter units have small spurious high frequency responses which are removed with the active multiple feedback net-

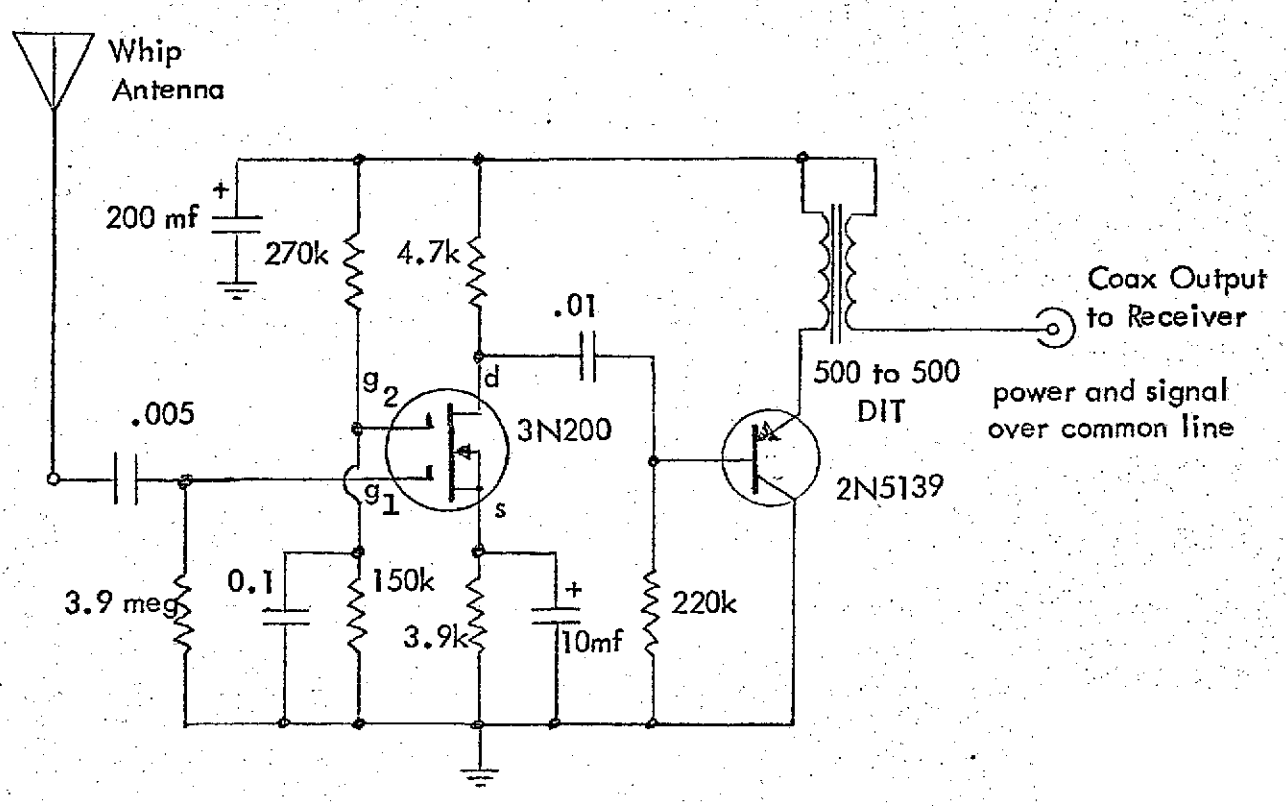


Figure 4. Wide Band Preamplifier. (10db gain, 1.5 - 150 KHz)

work of Figure 6. The lowpass filter is designed with a cutoff of 4 to 5 times the operating VLF frequency, based on an output impedance of about 25 K ohms for the ceramic filter as the input source to the filter. The ceramic filters are "tuned" to the exact OMEGA center frequency with series capacitors for which they have a very low sensitivity factor of about 0.1 Hz/pf. Each amplifier is designed for low phase error or exactly 180° at the frequency of interest. Very similar amplifiers may also be used on other VLF channels such as for the high power communications channels around 17.8 KHz and the time-frequency standard station WWVL on 20 KHz or WWVB on 60 KHz.

The system bandwidth is further reduced in a second stage nearly identical to the first stage filter. This results in the very narrow bandpass curve of Figure 7 with good skirt selectivity. The two stage filter is designed for an overall gain of slightly greater than 20 db for a whip antenna usage. For OMEGA use it is often desirable to have a two channel receiver or filters for both the 10.2 KHz and 13.6 KHz frequencies as shown in Figure 8. Here a single quad LM 3900 provides both pairs of amplifiers with reasonably good isolation on a simple layout illustrated in the front part (antenna terminal or preamp output) of the assembly photograph of Figure 9. The very early narrow bandwidth reduction characteristics in two stage jumps results in reasonably good performance even in noisy situations with a whip antenna.

A primary goal is the phase measurement of the signal and a means for determining the zero crossings of the signal frequency. A standard FM limiter-detector integrated circuit package normally used at 10.7 MHz, turns out to provide both good limiting properties with no phase error as well as a means of measuring signal amplitude. Some amplitude information is desirable so that the local receiver clock may be easily synchronized to the transmitted OMEGA format by using the strongest station burst for lock-up when the receiver is first turned on. The circuit is shown in Figure 10. The bandlimited output for phase information is taken just ahead of the multiplier. A reference voltage is also available on the same chip for use in a comparator with the DC level of the reference the same as the average DC level of the signal output.

The multiplier provides a synchronous product detector using the unlimited filter output driving an emitter follower to isolate the relative high filter output impedance of 1000 ohms or so from the multiplier input terminal. This envelope detector has a characteristic such as illustrated in Figure 11. The overall gain from antenna input to limiter output is 104 db for this graph. Thus the threshold starting around 3 microvolts is about 10 db lower than the normal atmospheric noise level at the antenna in this 15 Hz receiver bandwidth. This results in a compression action or hard limiting wherein signals from 10 microvolts to 10,000 microvolts all produce about 1.5 volts peak-to-peak amplitude signal output for phase measurements.

The envelope detector output level changes of typically 1 volt swing on a 300 microvolt signal provide a very satisfactory initializing envelope pulse for receiver start-up.

Still more system gain is used to provide clean square wave edges for further use. The limiter output signal drives the comparator and edge detector circuit of Figure 12. A small amount of decoupling at the limiter output (Figure 10) is needed to prevent a slight

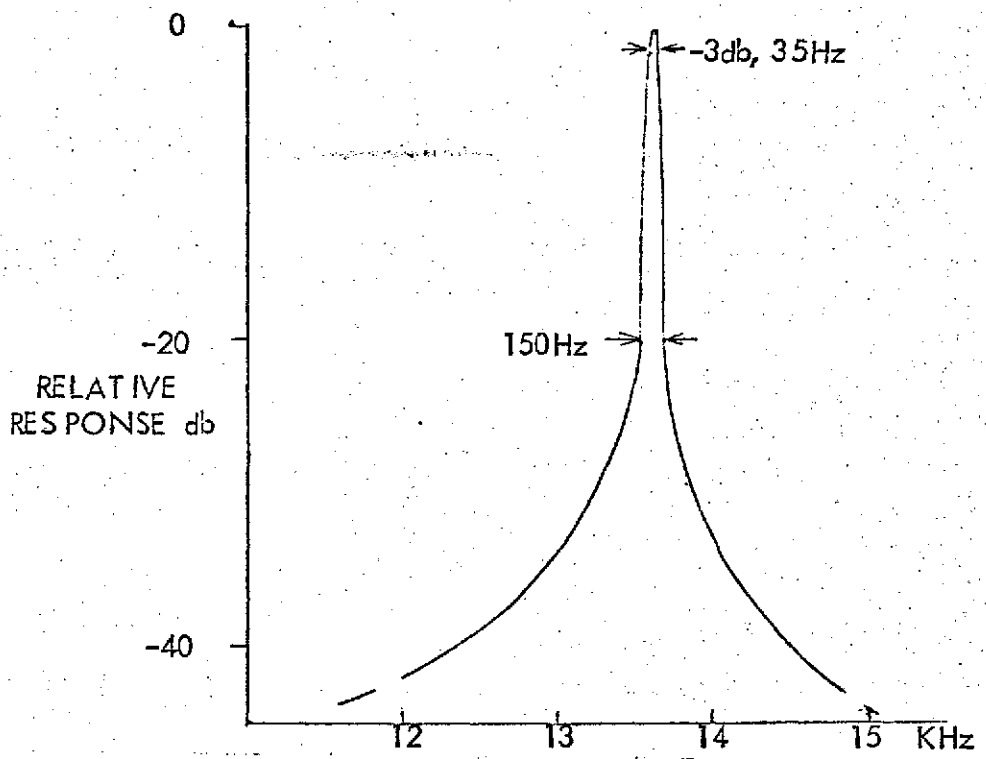
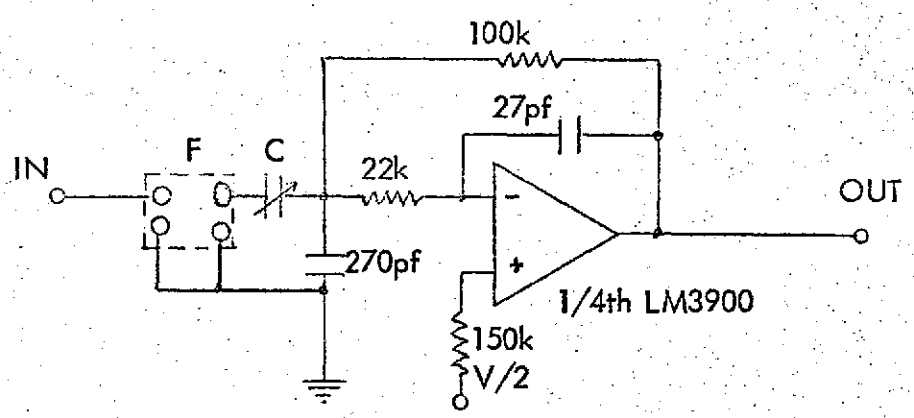


Figure 5. Single Stage Filter.



F Vernitron ceramic filter
LF-10.2B
LF-13.6B

C Tuning capacitor
~ 220pf at 10.2KHz
~ 120pf at 13.6KHz

Figure 6. Single Stage Filter Block.

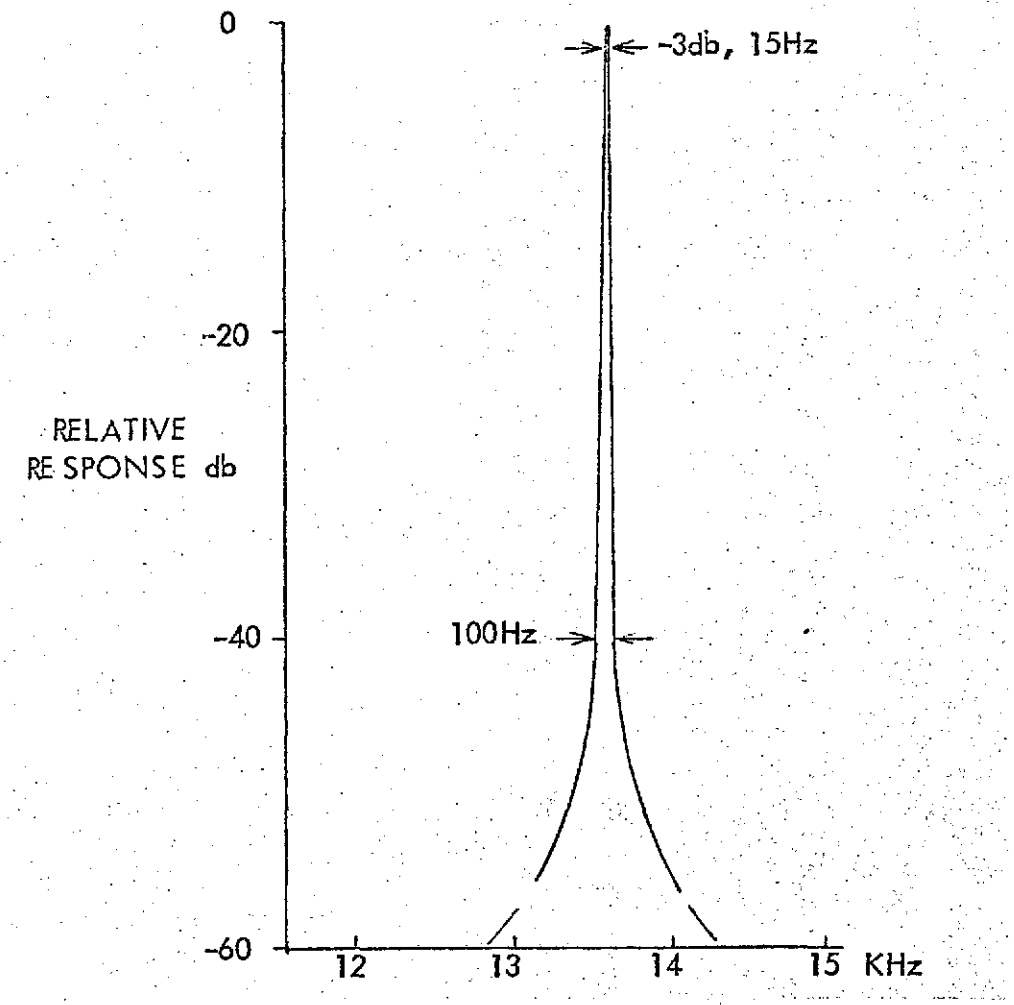


Figure 7. Two Stage Filter.

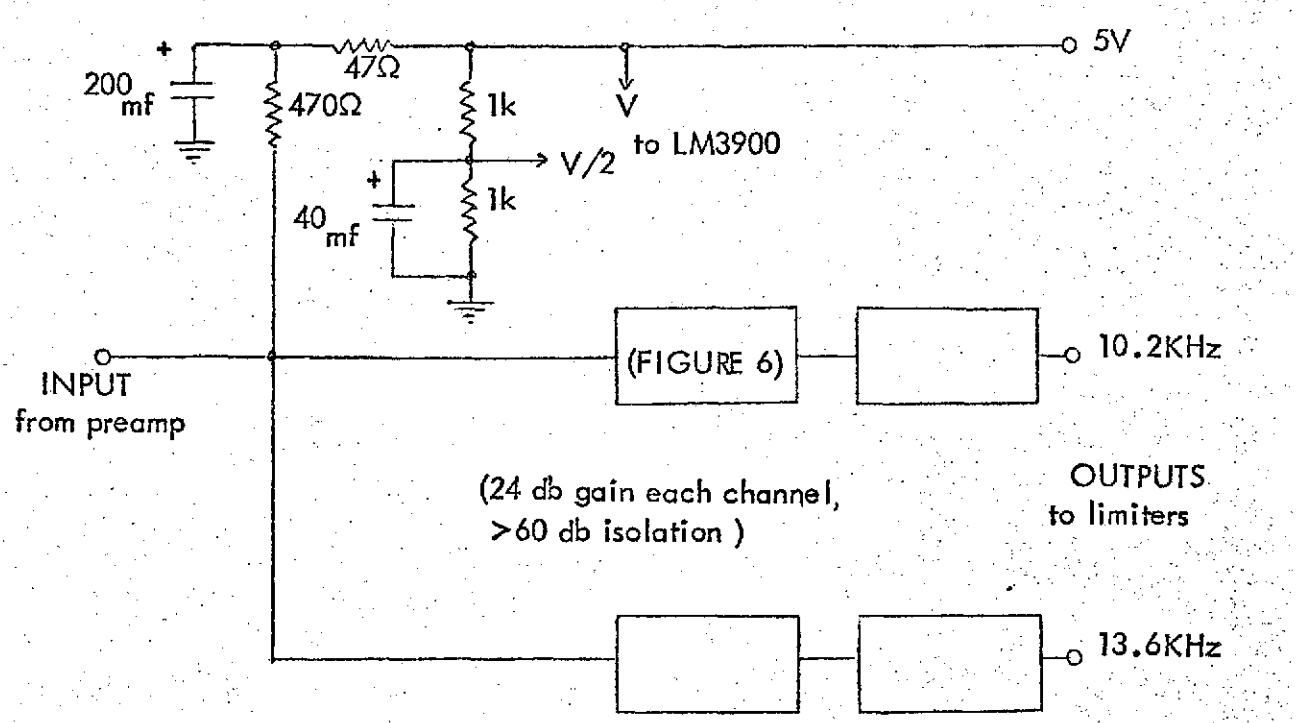


Figure 8. Two Stage, Two Channel Filter.

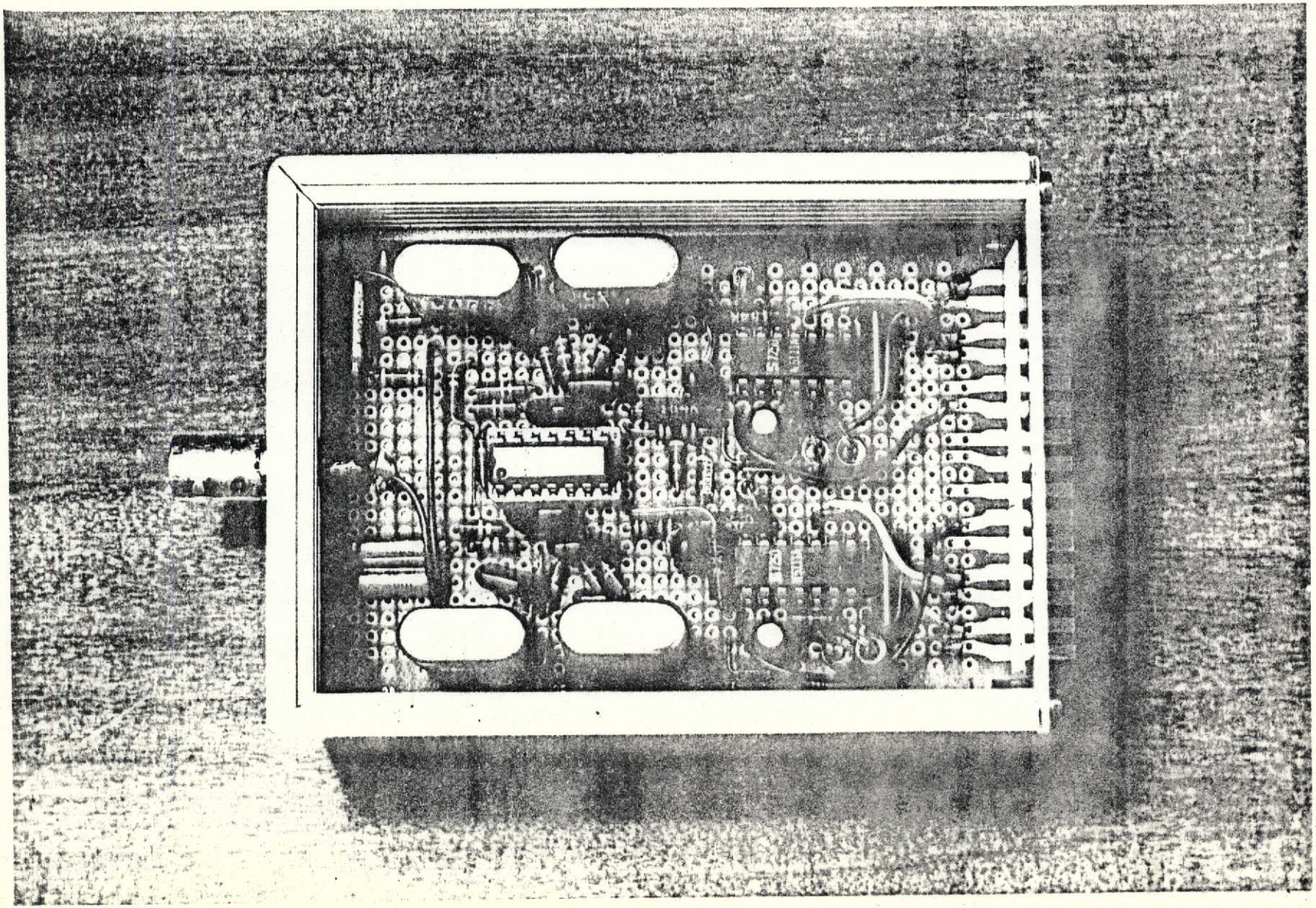
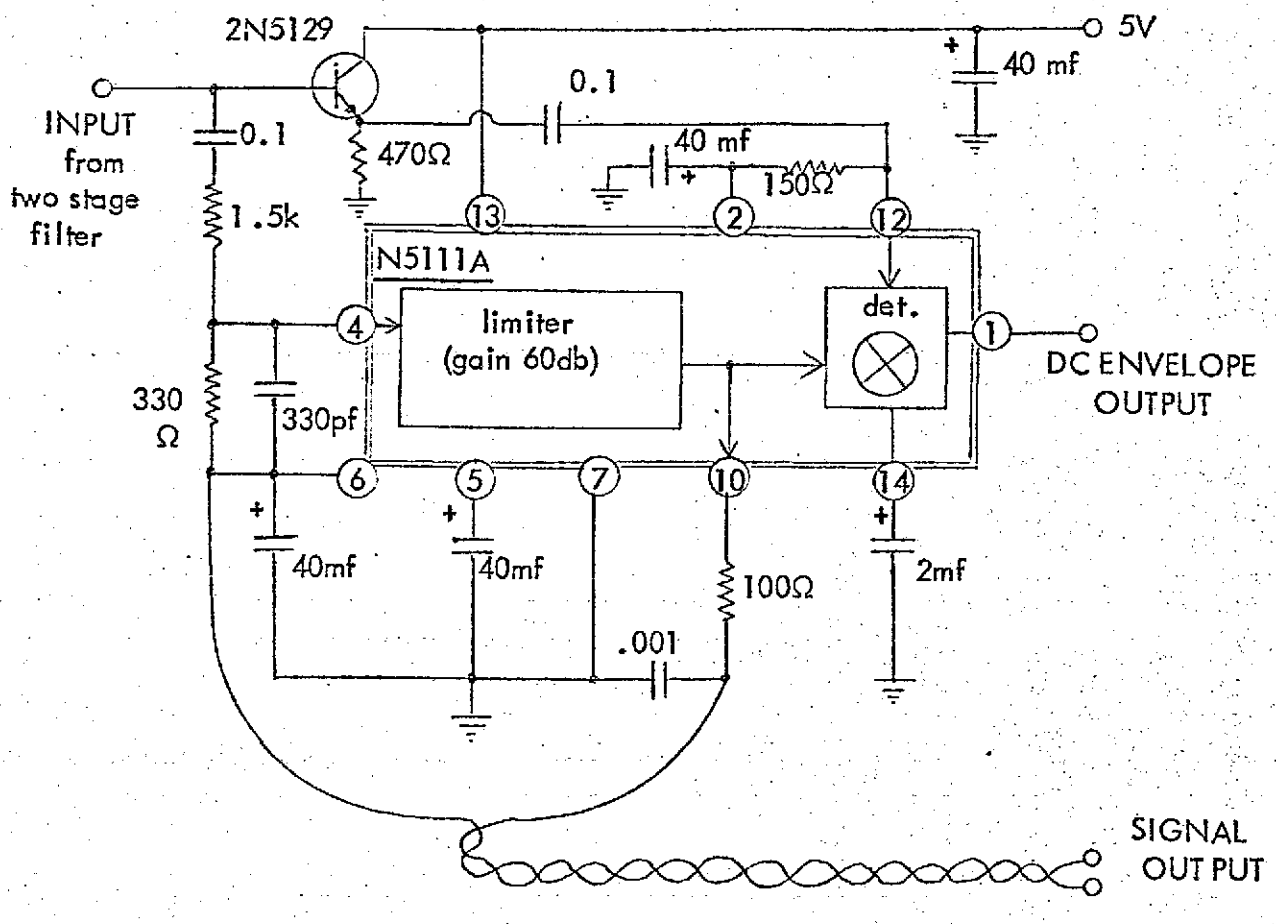


Figure 9. Photograph of Two Channel Filter-Limiter Assembly.



(same circuit for 10.2KHz, 13.6KHz)

Figure 10. Limiter - Envelope Detector.

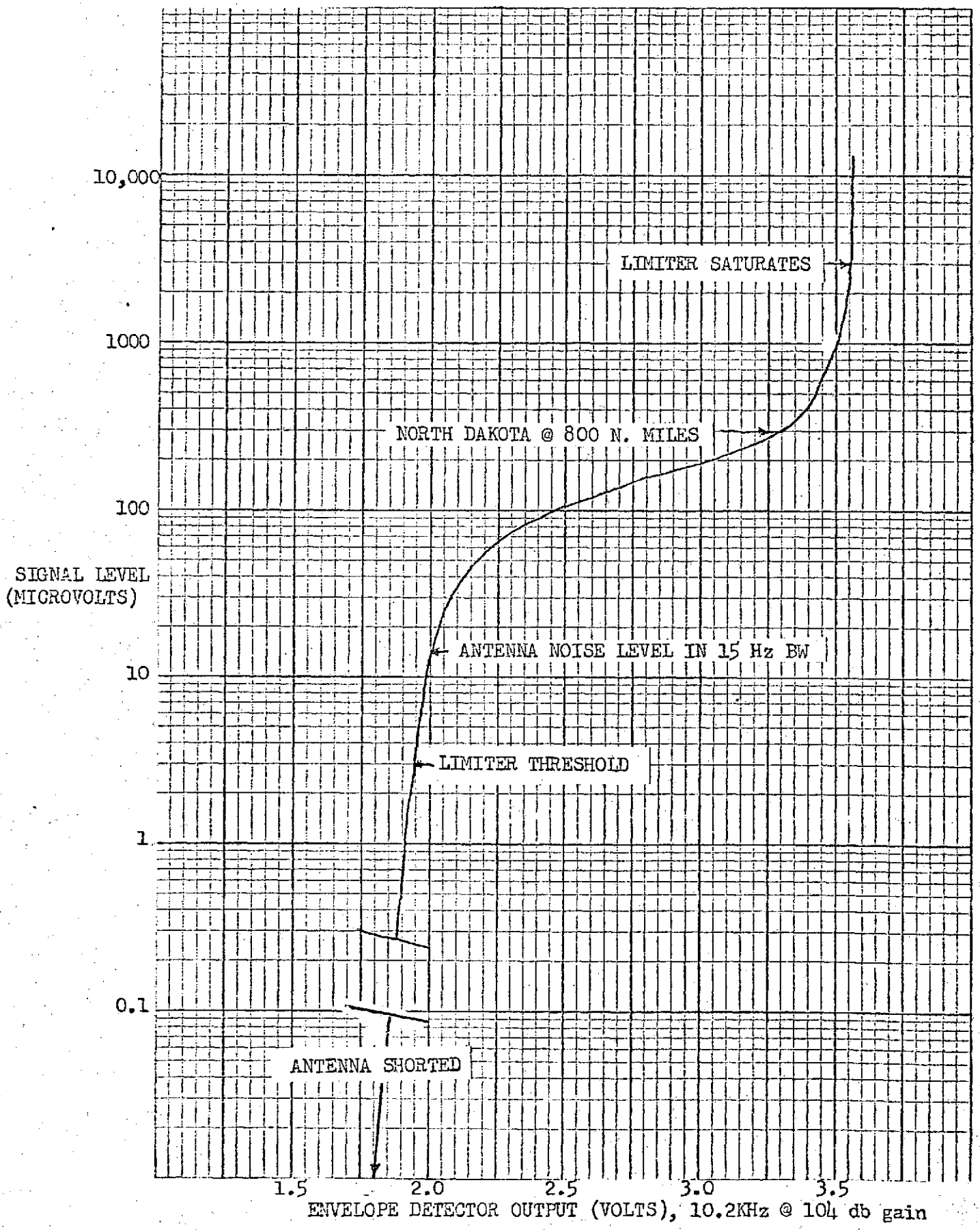


Figure 11. Envelope Detector Characteristics.

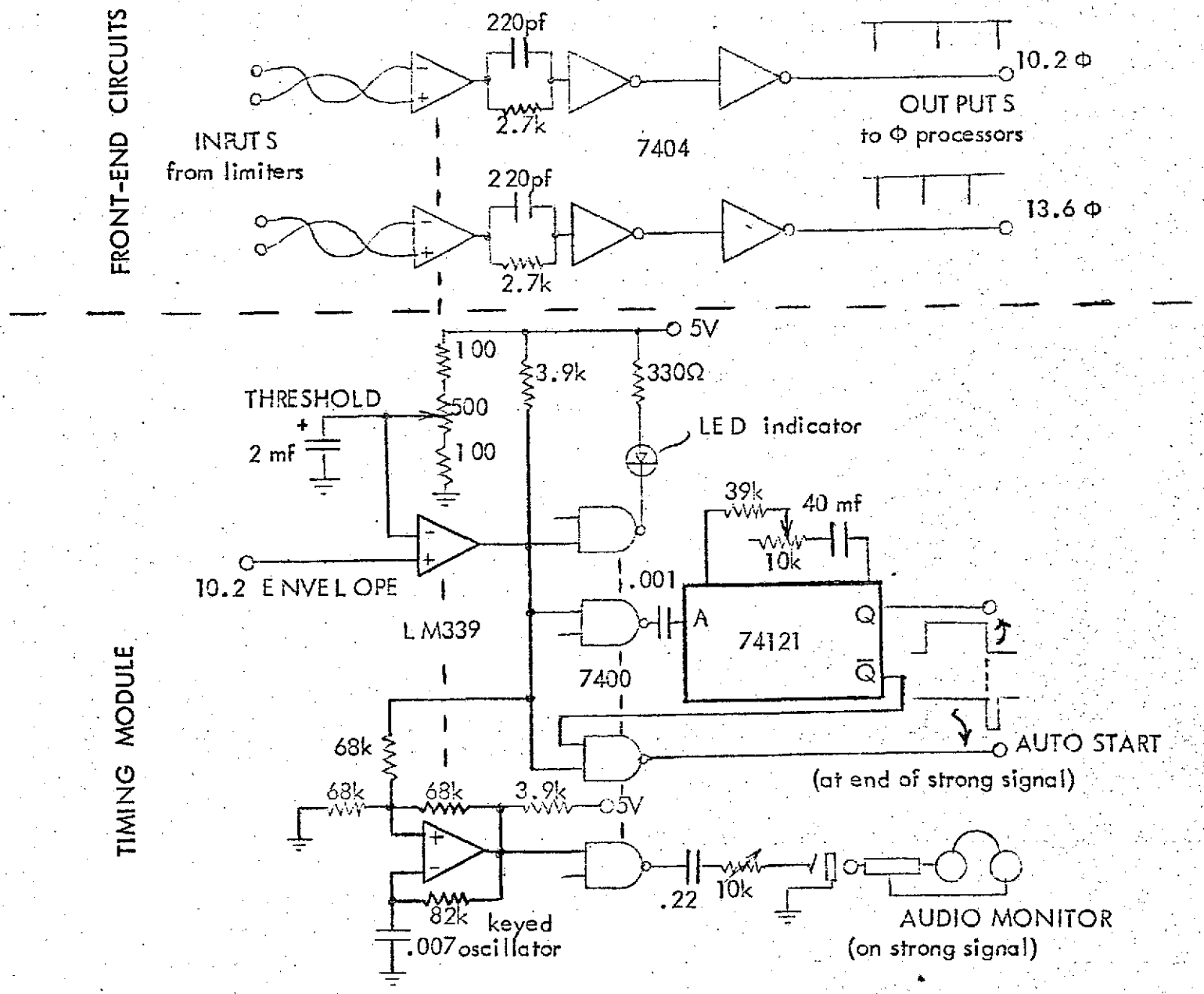


Figure 12. Zero Crossing Detectors and Strong Signal Monitor.

tendency for regeneration due to the very high frequency gain in the limiter circuit (the limiter provides 60 db gain). The phase shift introduced by the decoupling is smaller than the least significant increment of phase measurement desired, or smaller than 3° at 13.6 KHz. The comparator drives the edge detector differentiator which provides a simple means of generating pulse trains for the leading edge zero crossings of the original signal. The comparator circuit provides an additional 20 db or more of compression, resulting in measurable square waves for signals down to 1 microvolt at the preamp input.

Figure 12 also illustrates the use of the envelope output for generating an auto start pulse at the end of the strongest signal burst. For a major portion of North America, the 10.2 KHz signal from D channel at North Dakota will provide a strong signal level of greater than 100 microvolts at a whip antenna. The envelope output is fed to a comparator with a threshold adjustment to provide a pulse proportional to the length of the envelope output. The width of the D channel signal as seen by the 15 Hz bandwidth filter will be around 1200 ms but slightly delayed due to the filter bandwidth and the envelope filter round off capacitor of Figure 10 (2 mfd). A monostable (74121) adjusted for an output width of about 1150 ms is compared in a NAND gate with the comparator envelope output. This results in a short pulse, 50 ms or less, near the end of the D channel signal. The slight delay and exact width are not important since the receiver synchronizing circuit to be described later, will tolerate a 50 ms error. This auto start pulse is used for later synchronization of the local receiver clock. The same comparator circuit also drives a visible LED indicator and keys an audio oscillator for qualitative monitoring of the strongest signal. The audio monitor is quite useful to tell the pilot or navigator that his receiver is indeed receiving signals. Both the audio signal burst and the LED may be observed flickering between signals on noise pulses but a strong indication could be obtained on the D channel virtually anywhere in the USA depending upon the adjustment of the threshold control. The audio start pulse is only required once for initial startup when the local receiver time takes over, but is continually operating to provide these qualitative signal level monitors. Using a combination of both width and amplitude discrimination provided by this circuit, it should be possible to generate synchronizing events for other stations in the OMEGA system within 1500 nautical miles or farther from the station chosen.

The receiver front-end modules documented here were completed under the third-year NASA program, and they form the basis for receiver processing of Omega signals to recover the nagivation information. Initial experiments with various forms of signal processing techniques (including signal averaging and digital phase-lock loops) indicate that sufficient signal exists for later processing. Therefore, no major changes are anticipated in the receiver front-end modules during the fourth-year effort.

D. Receiver Timing Modules

All OMEGA receiver systems require some form of internal clock to provide a means of telling which station is being measured at a particular time. A variety of methods are used, most of which also provide internal housekeeping and phase measurement references

from the same clock. The more sophisticated processors use cycle matching systems with a signal reference oscillator operating at a high enough bit rate to generate all possible signals of interest from 0.1 Hz, the time interval of one complete OMEGA sequence, to 10.4448 MHz which is a 10 bit clock rate for a 10.2 KHz signal.

$(2^{10} \times 10{,}200 = 10.4448$ MHz or better than 1/1000 of a 10.2 lane)

Professor Pierce of Harvard in designing the original system, chose 408 KHz as the least common multiple frequency of all the signals of interest. In the simpler receivers, one or two of the 3 channels available are used. If we consider 10.2 KHz and 13.6 KHz, the least common multiple frequency is 40.8 KHz ($10.2 \times 4 = 13.6 \times 3 = 40.8$). A 6 bit resolution of 10.2 KHz lanes requires a clock rate of $2 \times 10.2 = 870.4$ KHz.

If we are trying to use a common clock frequency, it is of interest to consider the very minimal processor rate required for a specified bit precision in the final output displays. A 6 bit 10.2 KHz clock rate will provide 1/64th of a lane resolution.

Some commercial OMEGA receivers use a final output display precision of 1/10th of a 10.2 lane. Thus each output increment of phase represents slightly less than a mile on the pair baseline. The noisiness of the OMEGA raw data generally makes it undesirable to present information to the pilot at a centilane or 1/100th of a 10.2 lane precision. The data, even when averaged over a few time slots, will be varying too much, particularly if one of the stations of the pair is a weak signal. Thus one-half to one mile output increments of phase are desirable for navigational use to aid in smoothing the information display for the pilot or navigator.

In order to supply the data readout at this precision it is usually necessary to provide higher phase processing accuracy. Commercial receivers may typically use 8 bits at 10.2 and 13.6 KHz, or 1/256th of a lane. The processor methods described here use 6 bits for processing and 4 bits for readout providing a readout equivalent of 1/16th of a 10.2 KHz lane. The internal processing is at a 6 bit 10.2 KHz level which is effectively 1/64th of a 10.2 lane. Since cumulative difference methods are not used in this lower cost approach, the 6 bit precision in processing provides sufficient accuracy for a reasonably low quantization error at the 4 bit output level. The 652.8 KHz clock frequency is actually easier to implement at a higher crystal frequency of say $10 \times 652.8 = 6.528$ MHz because of better oscillator stability and lower crystal costs. Thus a clock at 6.528 MHz or some other simple integer multiple of 652.8 KHz is the first requirement of a timer system for a simplified binary processing OMEGA receiver at 10.2 KHz.

As discussed throughout this paper, we desire to stress generality plus low cost in the OMEGA receiver. Therefore, some effort will be made during the fourth-year program to achieve a receiver master clock which can be used both at 10.2 and 13.6 KHz and which is stable enough to permit direct measurements on Omega signal phase in a backup mode operation when three stations are not available for true hyperbolic Omega navigation. The navigation options which are being considered for back-up use are sum-and-difference

Omega navigation and direct-ranging navigation. Both methods use only two transmitting stations, and both involve direct measurements of Omega against the receiver clock. True hyperbolic Omega navigation, by comparison, involves a subtraction of two phase measurements in which the clock's long-term instability cancels out.

One method currently in breadboard form uses an oscillator at 5 MHz, offering at least stability of 1 part in 10^7, to drive a chain of binary-coded-decimal rate multipliers, as illustrated in Figure 13. An oscillator offset error of 1 part in 10^7 offers less than 1 bit error in 8 bits (1 part in 256) when measuring at 10.2 KHz and assuming phase measurements within 3.6 seconds. Measurements of Omega pairs such as B-C and B-D take place well within this 3.6 second time frame. The proposed 6-bit processing accuracy places an even less stringent criterion on the oscillator stability, when the receiver is operating in Omega hyperbolic mode. Direct-ranging measurements, of course, place much more importance on stable master clock frequencies, since errors are not cancelled during processing of navigation data.

The 5 MHz oscillator of Figure 13 is divided by 0.52224 in the rate multiplier chain to yield 2.6112 MHz. This frequency is 64 x 408 KHz, or the common multiple of 10.2 KHz and 13.6 KHz with a multiplier of 64 to provide 6-bit precision. Division of the 2.6112 MHz by 4 yields 652.8 KHz, or 10.2 KHz x 64. Division by 3 gives 870.4 KHz, or 13.6 KHz x 64. Use of one of these output frequencies to drive the digital phase-lock loop, described in the next section, causes the receiver to operate at the appropriate Omega frequency. Other operating frequencies are possible through suitable programming of the decades in the rate-multiplier chain and by providing the appropriate front-end filter.

It should be noted that the output of rate multiplier chains is an asymmetrical waveform which contains the correct number of pulse edges in each second, but whose duty cycle varies somewhat from pulse to pulse. There is, therefore, some inherent phase jitter in the out-put wave. Through post-division by 3 or 4, as discussed above, and by insertion of a crystal filter at 2.6112 MHz if necessary, we feel such jitter will be reduced to an acceptable level. This jitter level will, of course, be one of the points of emphasis in the evaluation of the rate-multiplier clock circuit.

We feel that the rate-multiplier clock offers improved stability at low cost and with relatively uncomplicated circuitry. The compatibility of the 5 MHz reference frequency with existing atomic clock standards will allow the receiver base to be used in high-precision measurements in addition to TCXO operation for most flight applications. The added stability will allow the use of range-range and phase sum-and-difference navigation methods as backup modes to the normal Omega hyperbolic methods. The digitally-programmable nature of the rate-multiplier chain offers generality for more sophisticated applications in the future such as frequency-hopping operation or use with communications VLF stations or Russian Omega-like signals.

Another method for generating master clock frequencies has been investigated during the third-year NASA Tri-University effort at Ohio University. Technical Memorandum

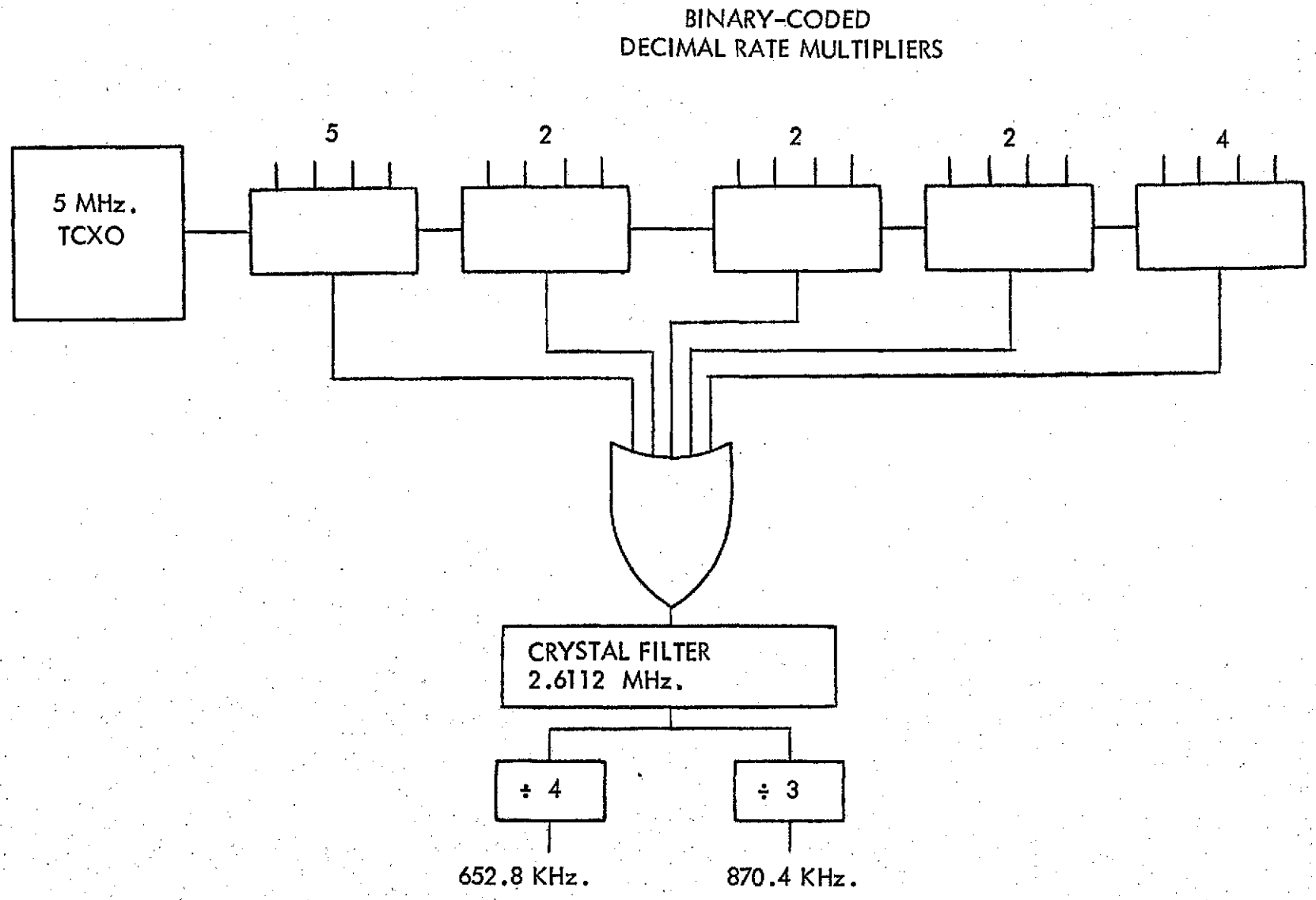


Figure 13. Rate-Multiplier Frequency Synthesizer.

NASA-6, "Phase-Lock Loop Synthesizer for Omega Reference Frequencies," by Kent Chamberlin, April, 1974, discusses the use of analog phase-lock techniques for generation of 4080 KHz, or ten times the common multiple frequency at 10.2 KHz and 13.6 KHz. This circuit uses the 5 MHz reference frequency which is desired for generality and uses digital dividers to accomplish the loop filtering requirement.

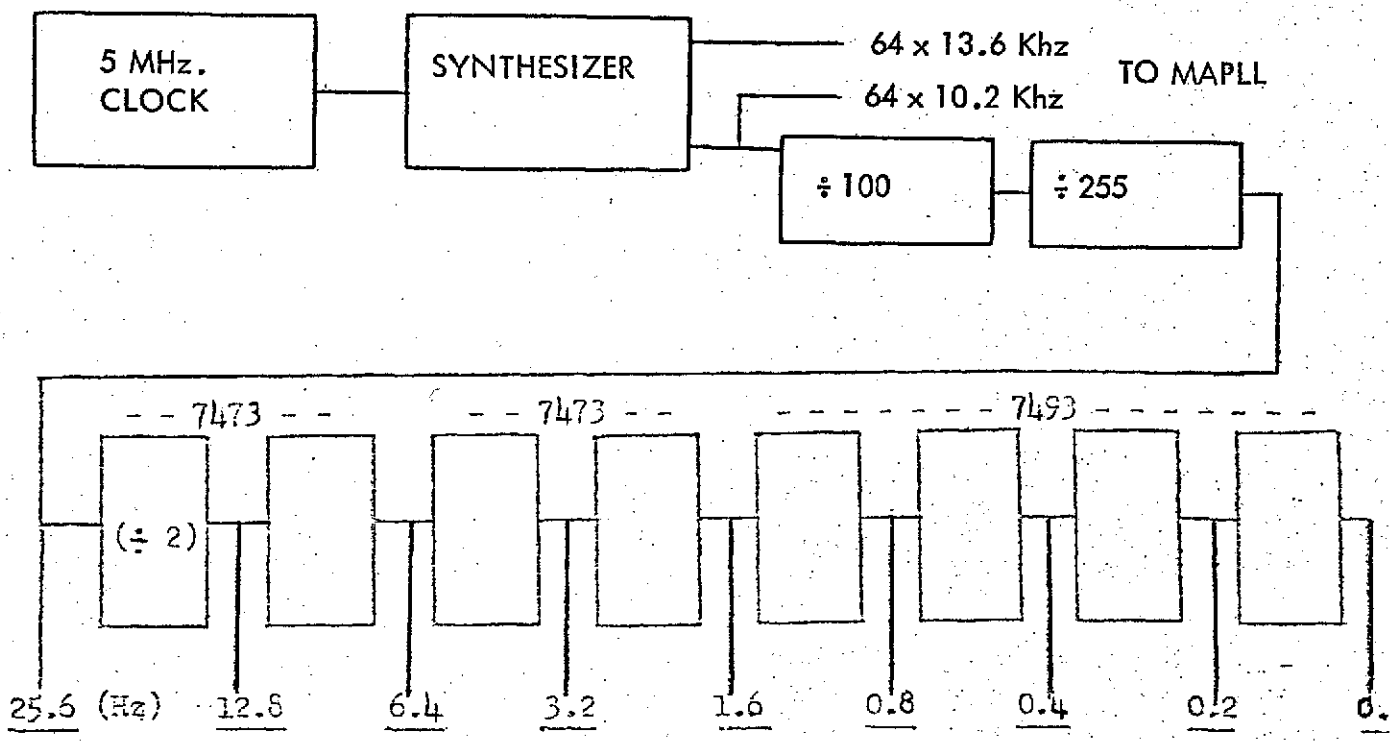
The synthesizer output is provided both to the reference counter of the digital phase-lock loop, discussed later, and to the "housekeeping timer" circuitry (HKT). The HKT uses the 64 x 10.2 KHz synthesizer output to generate all necessary receiver pulses for phase count enable, receiver channel control and the 0.1 Hz Omega decommutator timer. See Figure 14.

An octal decoder generates a gate proportional to time slot position, and logic gates (not shown) generate the timing functions illustrated in Figure 15 . In order to start this circuit in synchronism with the OMEGA sequence, a uniform time slot scheme is used. Uniform length time slot read and write intervals are far easier to generate than cycle matching to the OMEGA sequence. If a delay of 1.25 seconds/4 is used after the station selected for startup, all of the uniform sample intervals occur when Omega stations are transmitting.

The semi-automatic startup circuit is illustrated in Figure 16 . Here a no-bounce push button circuit is used to provide a reset signal. The reset button is activated after receiver turn on and after the threshold control for signal envelope is adjusted for blinking every 10 seconds on the desired signal. This stops the decoder at count zero in the pre-selected C-D time slot position with D on 10.2 KHz. Within 50 ms. of the end of the next D signal, the circuit if Figure 16 latches up and starts all the divider chains of Figure 14 operating. The dividers down to 0.8 Hz are all preset to the complement of the divisor. When the auto start pulse comes on, they start counting immediately (within 1/6528000 seconds) and the 0.4 stage flips over T/4 seconds later (where T = 1.25 seconds or 1/0.8 Hz).

In order to program for other start points, the position of the desired start on zero decoder output is shifted to the corresponding station pair. Effectively the D channel is permanently wired for startup. Shifting the start time to another channel is only a problem of relabeling the switches and indicators. Figure 17 illustrates the sequence indicator and switches for selecting the station pairs labelled for a start point on D channel at 10.2 KHz for the zero count of the decoder position. The sequence indicator is useful to monitor where the receiver is, at a particular time and also check to see if the D channel light comes on when the envelope blinker light is operating. Once started the circuitry continues to operate until it is shut down or the reset button is pushed for a new start. The circuit will operate for more than 24 hours continuously with no time slot sampling error overlap if the input clock frequency is set to within 1×10^{-7} or so.

More sophisticated housekeeping timer circuits with shift register methods are used in many commercial receivers. The direct divider-decoder timer illustrated in Figure 14



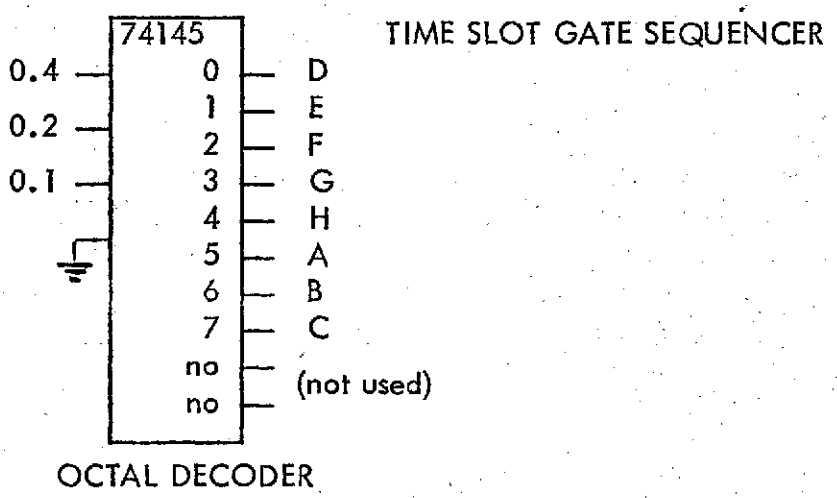


Figure 14. HKT Circuits.

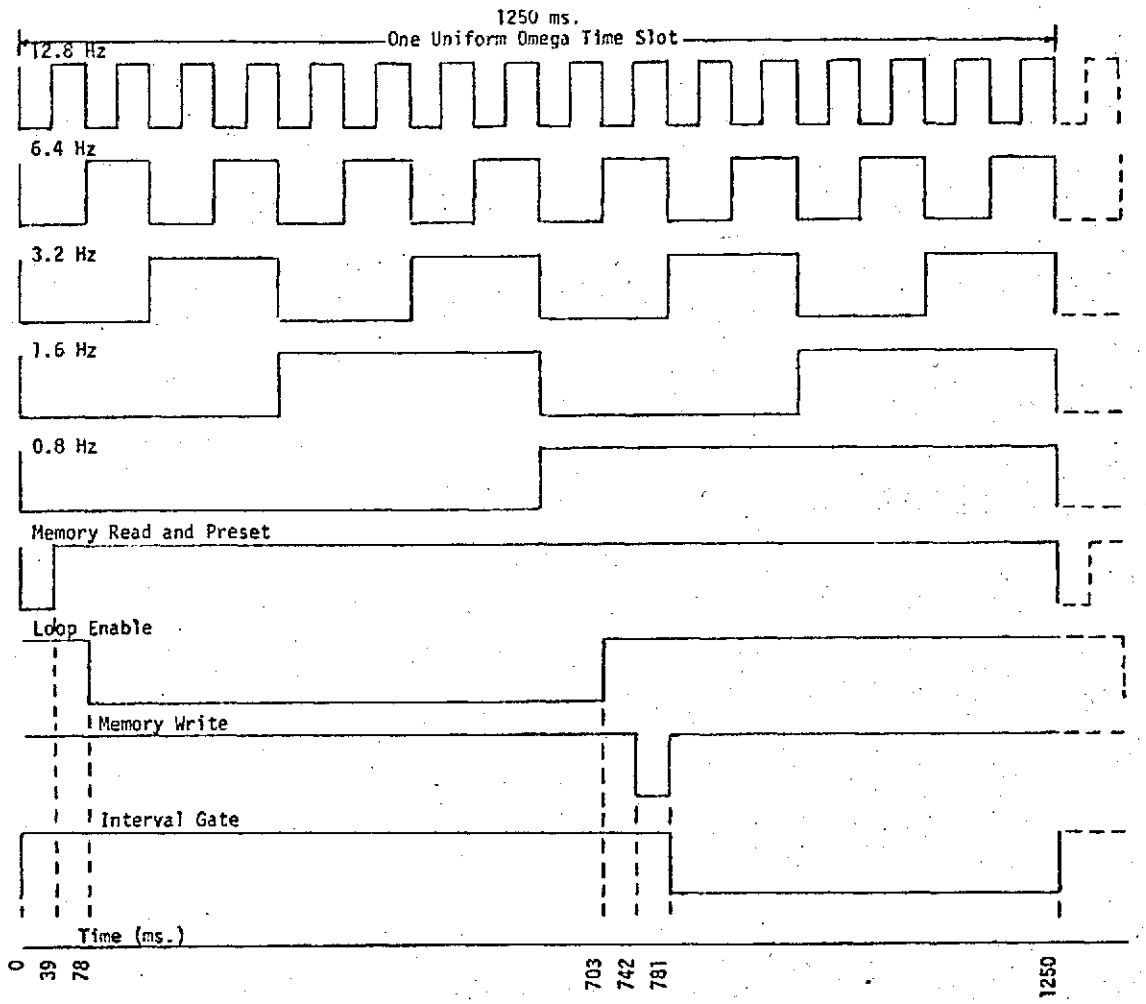


Figure 15. Receiver Timing Chart.

is quite uncomplicated within the limitations of readily available IC logic and MSI circuitry. Any other clock frequency chosen for other phase detection schemes will require about the same amount of hardware for these lower cost, uniform time slot sampling methods.

The HKT circuitry developed during the third-year NASA program will be retained for the receiver base, and the receiver clock will be replaced by a frequency synthesizer operating from a 5 MHz oscillator to gain stability and generality of design. The new clock will be capable of providing 10.2 KHz and 13.6 KHz reference frequencies simultaneously to allow receiver operation at either frequency, or in simultaneous-Omega mode, as desired for the application being investigated.

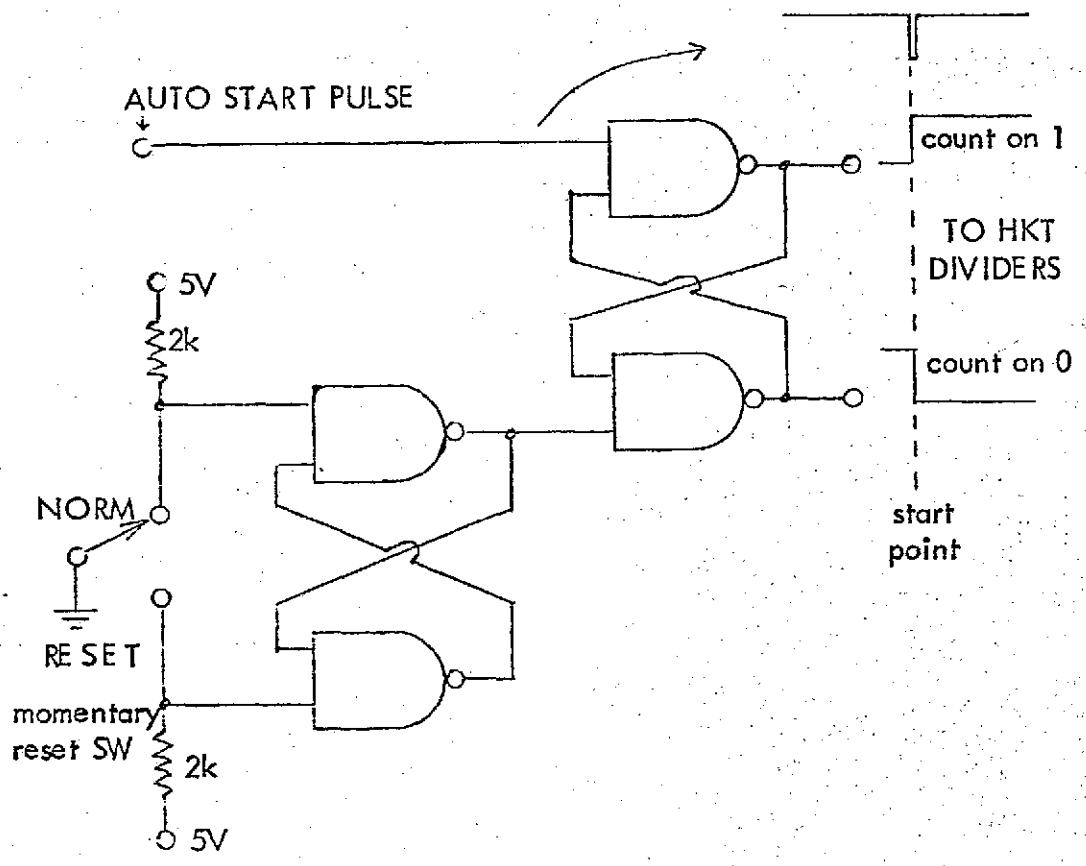


Figure 16. Start Circuit.

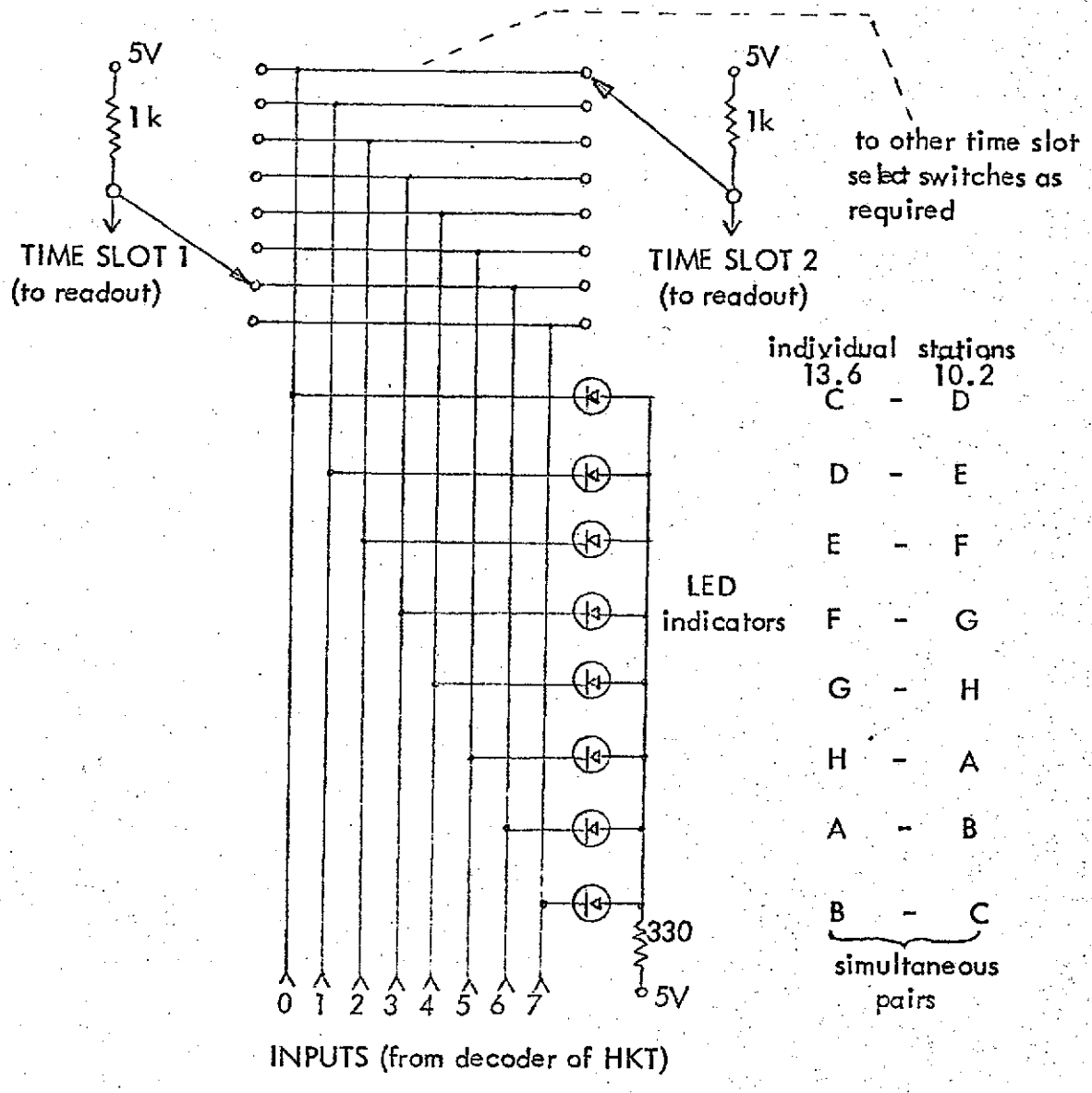


Figure 17. Station Select and Sequence Indicator.

E. Operation of the Memory-Aided Phase Lock Loop (MAPLL)

The block diagram for the MAPLL is shown in Figure 18. As shown, the 10.2 KHz Omega signal off the air and the locked 10.2 KHz are fed into a high-noise phase detector. This phase detector will increment the up count (thus advancing the phase of the locked signal) in the event that the Omega signal is ahead by less than half a cycle and increment the down count if the Omega signal is behind by less than 180 degrees. The phase detector timing diagram is shown in Figure 19.

This chart depicts a case where the incoming signals are in phase, although noise causes the Omega zero crossing to vary. The total cumulative count in the up/down counter after this sample would be zero, thus not altering the phase of the locked signal. If the phase of the incoming signals is dissimilar, the six most significant bits in the up/down counter will change after enough cycles have been sampled. The number of cycles required for this change of phase in the locked signal depends on both the number of low order bits not used for loop control in the up/down counter, and the signal-to-noise ratio. As would be expected, when no Omega signal is present, the up/down counting occurs principally in the lower order bits (which are not used for loop control) and the phase of the locked signal remains unchanged. This property is most beneficial in the event of a short term (several-time-slot) signal loss.

The phase of the locked signal is shifted by presenting two 6-bit data words to a comparator. One word cycles at a 10.2 KHz rate (a 6-bit counter will cycle at 1/64 the input rate) and the other (from the up/down counter) is constant within one 10.2 KHz cycle. It can be seen that the comparator will put out a pulse at a 10.2 KHz rate, its phase determined by the count in the up/down counter. The schematic for this circuit is shown in Figure 20.

MAPLL is, at this writing, in brassboard form. Measurements and computer simulations to determine desirable loop bandwidth and tracking characteristics are underway.

Preliminary observations indicate that the MAPLL offers decided advantages in sensitivity for the Omega receiver base. Emphasis during the fourth-year program will be placed upon completion of the loop design and optimization and on evaluation of its operation during laboratory and flight tests using existing Omega signals.

F. Memory Module

Of particular interest in the design of the digital phase-lock loop is the relatively easy transfer of phase information to digital processing circuitry so that navigation computations may proceed. Figure 21 illustrates the method for transferring eight channels of phase information (derived from the Omega time slots) to buffer storage for later use by the processor module.

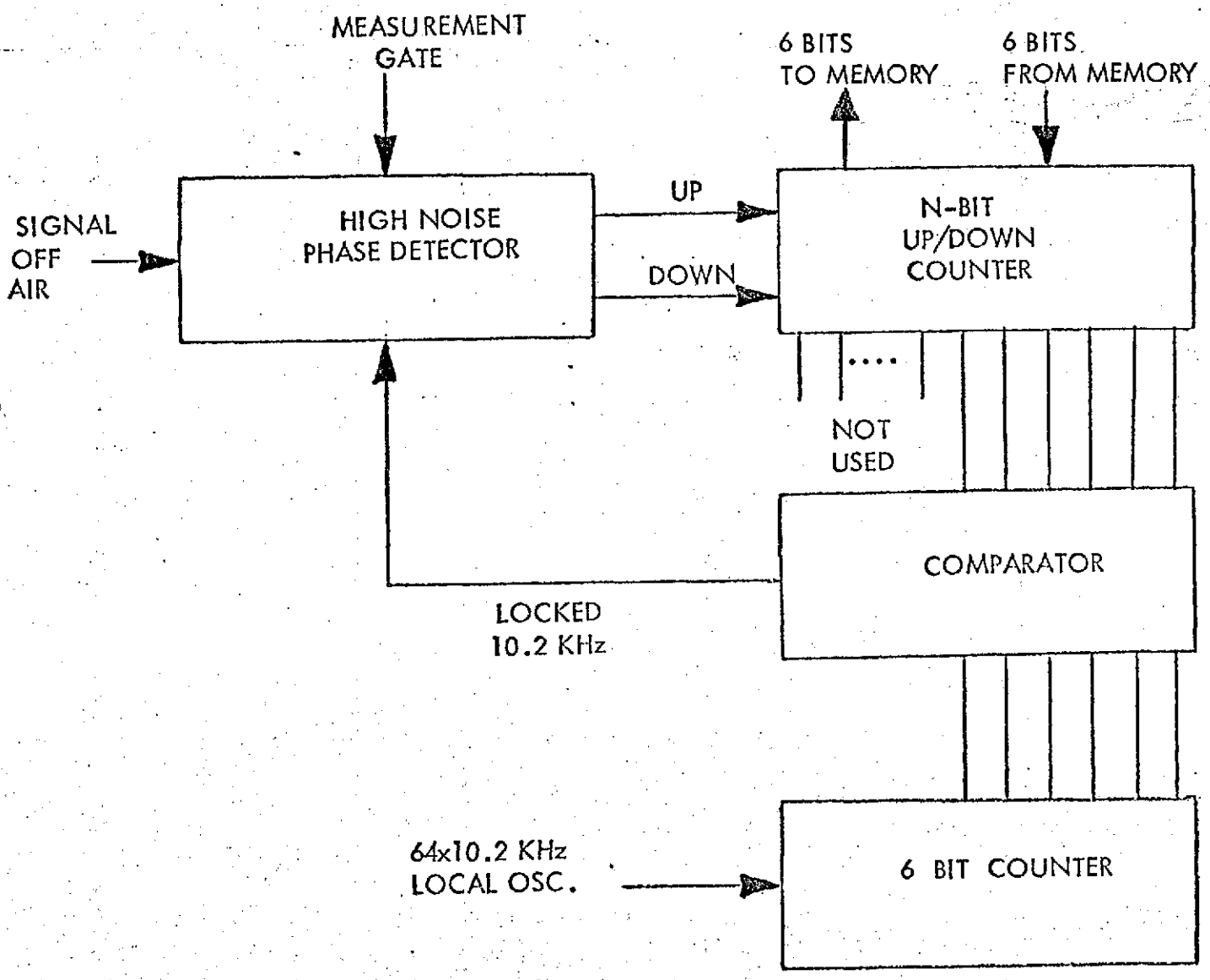


Figure 18. Memory-Aided Phase-Lock Loop (MAPLL).

PHASE DETECTOR FOR HIGH NOISE SIGNALS

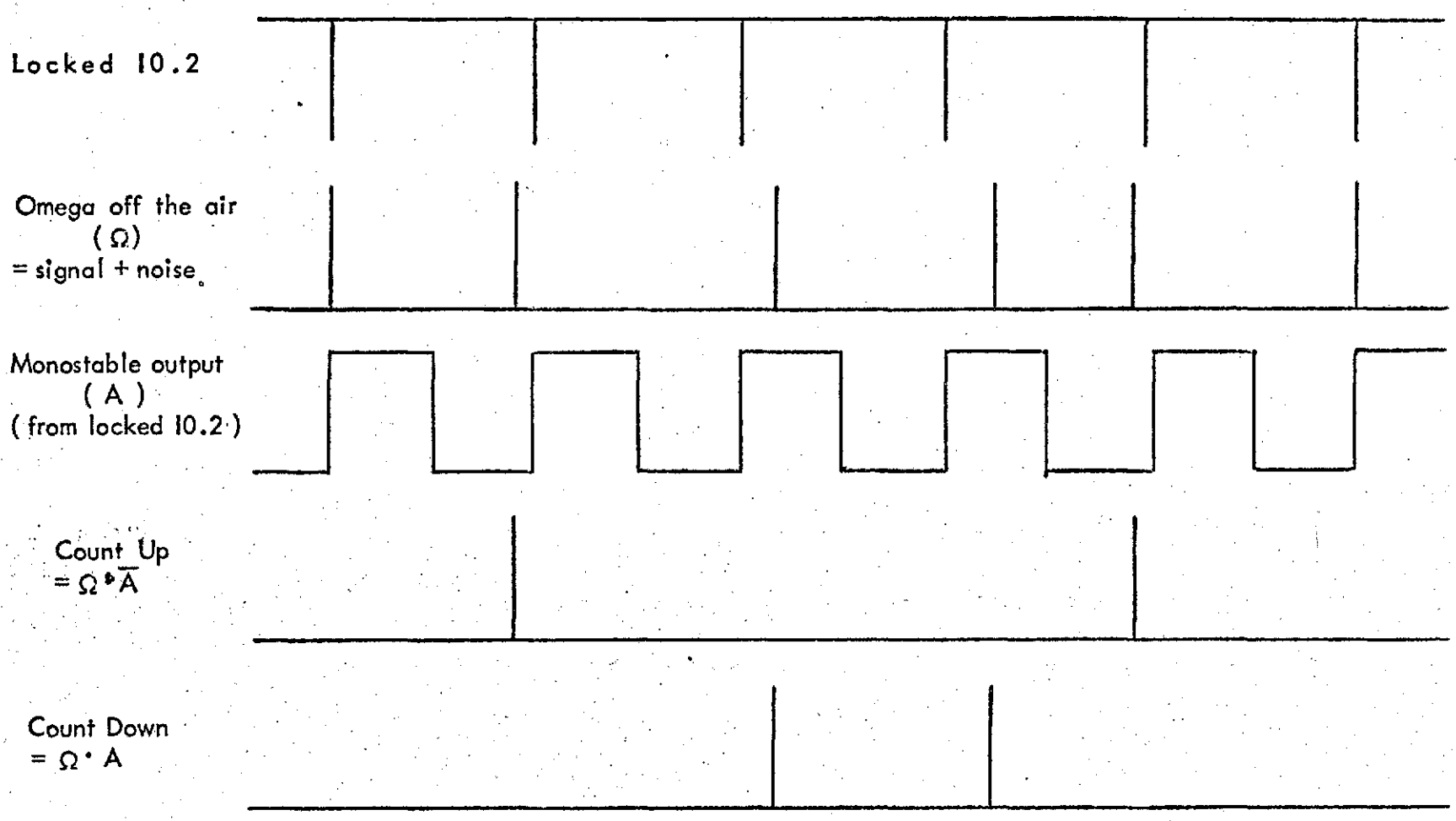


Figure 19. Phase Detector.

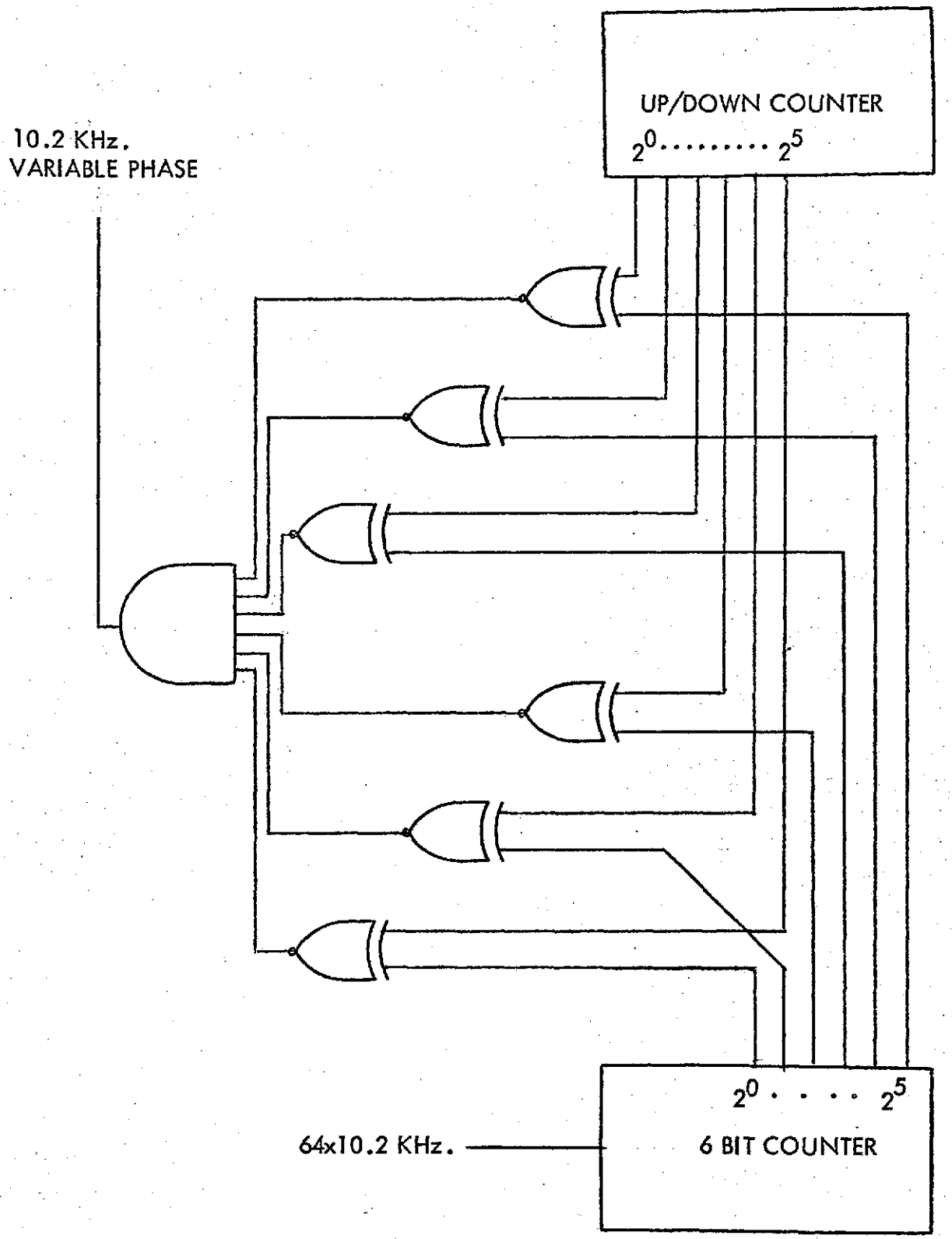


Figure 20. Digital Phase Shifter.

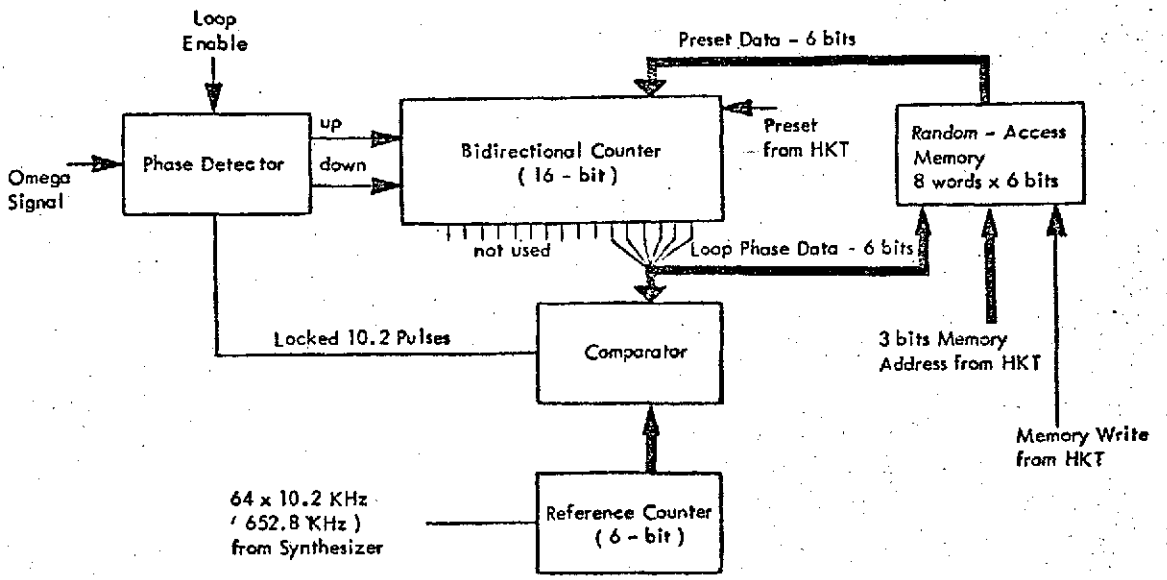


Figure 21. MAPLL Memory and Interface.

In Figure 21, the 6-bit counter, the comparator, and the up/down counter are parts of the digital phase-lock loop, described in the previous section. At the end of an Omega time-slot which is being measured, the up/down counter contains six bits of phase information as a result of the loop action during the time slot. This phase data is placed in the random-access memory at the address given by the octal time-slot address. When the time-slot address is advanced to the next slot by the HKT, the memory word addressed is read out of the RAM and placed in the up/down counter. In this manner, the loop is initialized with the previous phase measurement for the current time slot. The loop is then enabled so as to update the phase measurement with current Omega phase data.

The net result of the interface logic is to preserve all eight phase measurements from Omega signals and to prime the phase-lock loop for each phase measurement. By providing static phase outputs, each addressed by Omega time-slot, plus an interrupt which indicates that updated data is available, the interface offers facilities for (1) synchronous or asynchronous microprocessor access to Omega phase measurements, (2) the potential for microprocessor-updating activity, where one or more of the measures is reloaded by a microprocessor to aid the phase-lock loop during aircraft maneuvers, for example, and (3) sufficient integration in the loop to achieve narrow bandwidth while locking to Omega signals over multiple time slots.

III. APPLICATION MODULE: RECEIVER EVALUATION

As of this writing, one application module has been designed and constructed. This module, intended primarily to facilitate receiver tests and evaluation, receives as inputs from the Receiver Base:

A. Six bits of binary data (from MAPLL)

B. Four latch enable lines (from HKT module selector switches)

and produces as outputs:

A. One digital word (6 bits) per time slot for recording

B. Analog output of current phase reading in MAPLL

C. Analog output for LOP1 and LOP2.

Figure 22 outlines the evaluation module functions. Six bits of phase (current Omega time-slot versus receiver clock) are made available by the MAPLL up/down counter in each time slot. When one of the HKT selector switches is set to the current time slot, a latch enable pulse is sent to the 6-bit latch associated with the selector switch, at the end of the MAPLL count-enable gate for the current time slot. Thus, as data bits are sent to the MAPLL memory, they are also latched by the application module.

The two pairs of HKT selector switches allow the selection of two LOP's, each formed by subtraction of two Omega measures. Subtraction circuits are driven by the latch pairs, and the difference words drive DAC units to produce chart-recorder outputs of navigation data. Although not detailed in Figure 22, appropriate logic is included for computation of the two's complement of negative numbers, in the case B-C, for example, where the phase of B lags the phase of C.

Although such was not the primary motivation for production of the evaluation module, it happens that the functions provided are those required for navigation. With the addition of a lane-counter module, the receiver as described in this paper would contain all functions commonly found in small-boat Omega receivers. Taking the entire receiver sans lane-counter, less than $100 in integrated circuits are present, figured at the cost of such circuits in research quantities (5-10 items).

Figure 23 illustrates analog chart-recorded outputs from the application module made during a test flight from Athens, Ohio to Langley Field, Virginia. Aircraft heading was approximately 110° and airspeed was approximately 150 mph. These charts reflect the MAPLL integration time of 1/10 second. They contain no other signal integration.

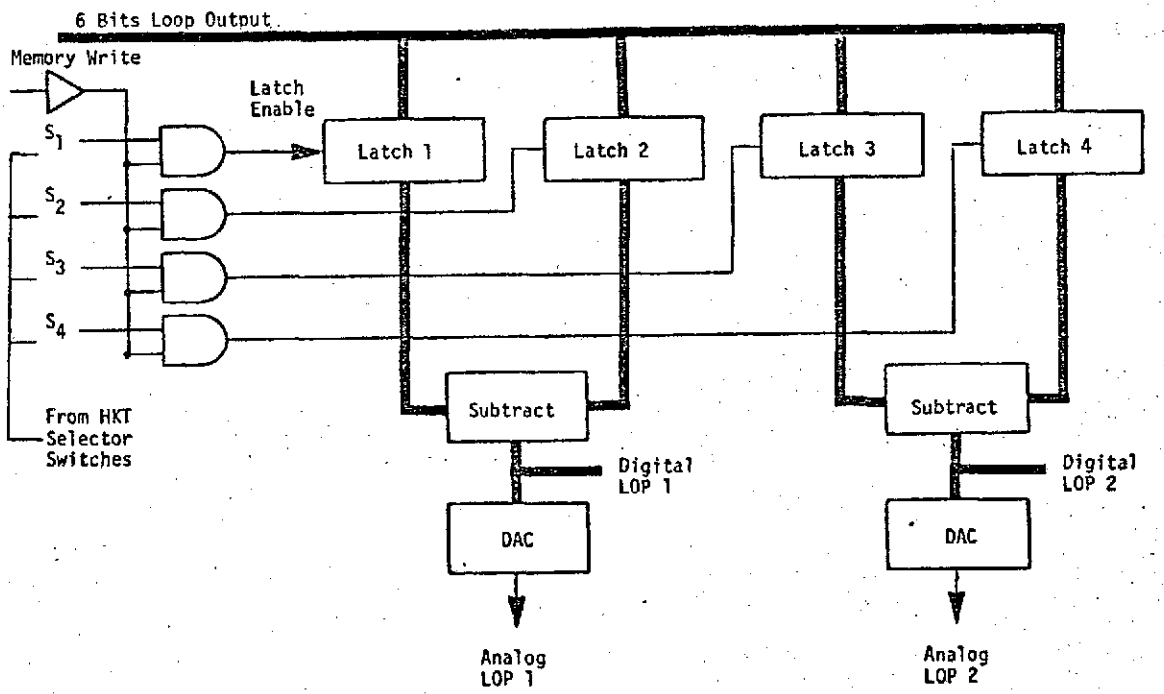


Figure 22. Application Module for Receiver Evaluation.

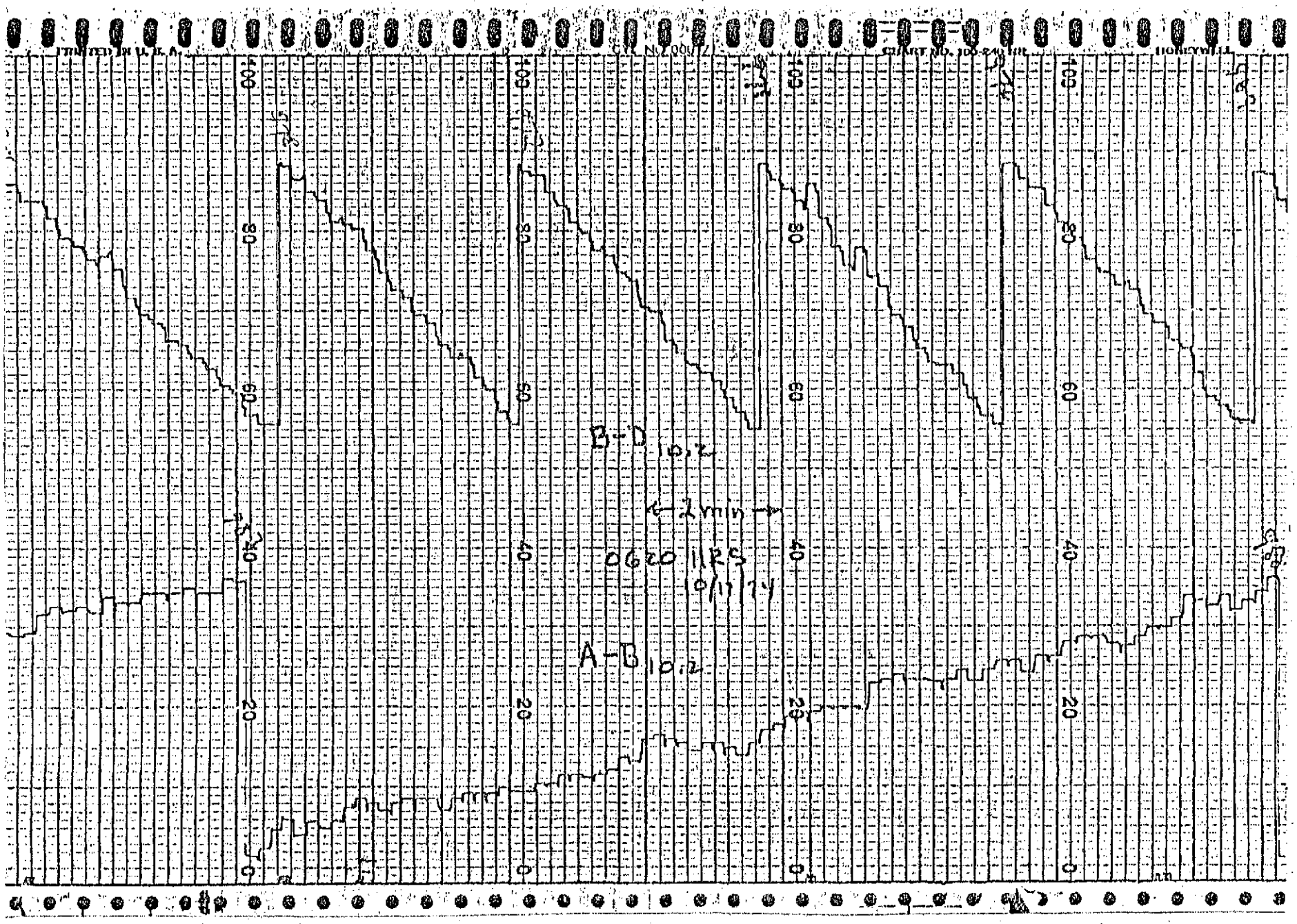


Figure 23. Analog Chart-Recorded Outputs from LOP Application Module.

IV. SUMMARY

The Receiver Base described in this paper is currently in brassboard form suitable for laboratory or flight experiments. Each module is being reviewed with the objective of adding noise-cancelling circuitry, minimizing digital integrated circuits to minimize cost, and increasing reliability wherever possible.

Three test flights have been conducted, with usable data acquired from each. Separate publications will be released to report results and provide for distribution of flight-test data to interested users.

The emphasis for future development of the Receiver Base is as follows:

A. Design and prototype a single-chip MAPLL unit.

B. Design a single-frequency, noise-cancelling front-end unit.

C. Implement a synchronous HKT module, eliminating all use of monostable multivibrators for stability and reliability.

D. Continue flight and laboratory data-collection activities.

V. ACKNOWLEDGEMENTS

This paper presents a status report on Ohio University's progress under the NASA Tri-University program in Air Transportation. By no means are all the ideas and advances reported herein my own. The contributions made through team effort toward the goal of a truly low-cost Omega navigation receiver are reported here in hopes of beginning the process of technology transfer from the laboratory to the user community. Each of the persons named below contributed individually to the total effort:

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